I claim:

1. A method of testing an integrated circuit, which comprises:

providing an integrated circuit that includes a self-test device;

starting to perform a test of the integrated circuit with the self-test device; and

subsequently, connecting the integrated circuit to an external testing device that performs a function selected from the group consisting of reading out results of the test and evaluating the results of the test.

2. The method according to claim 1, which comprises completing the test before performing the step of connecting the integrated circuit to the external testing device.

3. The method according to claim 1, which comprises at least partially completing the test while performing a function selected from the group consisting of temporarily storing the integrated circuit and transporting the integrated circuit to the external testing device.

4. The method according to claim 3, which comprises:

providing a self-test control device that causes performance of the test of the integrated circuit; and

moving the control device together with the integrated circuit.

5. The method according to claim 1, which comprises taking at least parts of the integrated circuit out of operation after the parts have been tested by the self-test device.

6. The method according to claim 5, which comprises:

with the self-test device, writing data into a test result memory; and

after testing the integrated circuit with the self-test device, taking out of operation, components of the integrated circuit that are not needed to continue to store the data in the test result memory.

7. The method according to claim 5, wherein the step of taking at least parts of the integrated circuit out of operation includes not supplying a clock signal, which is needed to operate the integrated circuit, to the parts of the integrated circuit.

8. The method according to claim 5, wherein the step of taking at least parts of the integrated circuit out of operation includes not supplying a supply voltage, which supplies the integrated circuit with power, to the parts of the integrated circuit.

9. The method according to claim 1, which comprises simultaneously testing a plurality of integrated circuits with the self-test device.

10. The method according to claim 9, which comprises providing the plurality of the integrated circuits on at least one wafer.

11. An apparatus for testing an integrated circuit using a self-test device that is located in the integrated circuit, which comprises:

a self-test control device for causing testing of the integrated circuit by the self-test device before the integrated circuit is connected to an external testing device that performs a function selected from the group consisting of reading out results of the test and evaluating the results of the test.

12. The apparatus according to claim 11, wherein said self-test control device is configured to complete the testing of the integrated circuit before the integrated circuit is connected to the external testing device.

13. The apparatus according to claim 11, wherein said self-test control device is configured to test the integrated circuit while allowing a function, selected from the group consisting of temporarily storing the integrated circuit and transporting the integrated circuit to the external testing device, to be performed.

14. The apparatus according to claim 11, wherein said self-test control device is constructed to be moved together with the integrated circuit.

15. The apparatus according to claim 11, in combination with the external testing device, wherein the external testing device tests aspects of the integrated circuit that are not tested by the self-test device, the aspects selected from the group consisting of components of the integrated circuit and functions of the integrated circuit.

16. An integrated circuit, comprising:

components;

a self-test device for testing said components; and

a device for, at a particular time, taking specific ones of said components out of operation;

the particular time selected from the group consisting of during the testing and after the testing.

17. The integrated circuit according to claim 16, comprising:

a test result memory for receiving data from said self-test device and for storing the data;

said specific ones of said components being ones of said components that are not needed in order to continue to store the data stored in said test result memory.

18. The integrated circuit according to claim 16, wherein said device prevents a clock signal, which is needed to operate said components, from being applied to said specific ones of said components.

19. The integrated circuit according to claim 16, wherein said device prevents a supply voltage, which is needed to

operate said components, from being applied to said specific ones of said components.

20. The integrated circuit according to claim 16, which comprises:

a test result memory for receiving data from said self-test device and for storing the data; and

a device for insuring that the data can not be changed after completion of the testing by said self-test device.

21. The integrated circuit according to claim 16, which comprises:

a test result memory for receiving data from said self-test device and for storing the data; and

a device for using the data stored in said test result memory to determine whether the testing has been completed.

22. The integrated circuit according to claim 16, comprising at least two different points for receiving voltages and signals that have to be supplied so that said self-test device can test said components.

23. The integrated circuit according to claim 22, wherein said at least two different points are electrically connected together.

24. A wafer comprising:

a plurality of integrated circuits that are configured for being separated apart by a subsequent cutting process;

said plurality of said integrated circuits are at least partially electrically connected to one another.

25. The wafer according to claim 24, comprising:

a wafer substrate; and

electrical connections formed by conductor tracks that are located on said wafer substrate and that electrically connect said plurality of said integrated circuits.

26. The wafer according to claim 24, comprising:

a self-test device located in said plurality of said integrated circuits;

said plurality of said integrated circuits including points to which signals selected from the group consisting of voltages and test signals must be supplied such that said self-test device can test said plurality of said integrated circuits.

27. The wafer according to claim 24, comprising:

a wafer substrate; and

electrical connections formed by conductor tracks that are located on said wafer substrate and that electrically connect said plurality of said integrated circuits;

said wafer substrate including contact zones that are constructed such that voltages and signals applied to them can be led onward, via said electrical connections to a number of said plurality of said integrated circuits;

said number of said plurality of said integrated circuits are selected from the group consisting of all of said plurality of said integrated circuits and some of said plurality of said integrated circuits.

28. The wafer according to claim 27, comprising:

a self-test device located in said plurality of said integrated circuits;

said contact zones including at least two different contact zones for receiving the voltages and the signals such that said plurality of said integrated circuits can be tested by said self-test device.